IN THE CLAIMS:

This listing of claims replaces all prior versions, and listings, of claims in the application.

1. (Currently Amended) A bus-repeater for coupling at least one first bus to a second bus, by way of which data are transmitted as serial digital signal pulse sequences, comprising at least one first and a second transmit-receive means, to which the first and, respectively, the second bus ~~may be~~ are coupled and by way of which the bus-repeater ~~may transmit~~ transmits signal pulse sequences received from the first bus to the second bus and vice versa, and locking means, which during the transmission of a signal pulse received by the first bus via the second bus lock transmission by the bus-repeater of signal pulses, received from the second bus, via the first bus for a lock time and vice versa.

2. (Original) The bus-repeater as set forth in claim 1, wherein the locking means are so designed that same prolong the locking time for a predetermined overrun time.

3. (Original) The bus-repeater as set forth in claim 1, comprising unloading means for unloading the first and/or the second bus after performance of transmission of a signal pulse to the first bus or, respectively, the second bus.

4. (Original) The bus-repeater as set forth in claim 3, wherein the unloading means include a clocked short circuit switch.

5. (Original) The bus-repeater as set forth in claim 3, wherein the unloading means are

adapted to be controlled by a voltage level, which is still present after the transmission of a signal pulse by the bus-repeater to the respective first or second bus.

6. (Currently Amended) The bus-repeater as set forth in claim 3, wherein the unloading means are activated at least during a part of ~~the~~ an overrun time and preferably during the entire overrun time.

7. (Currently Amended) The bus-repeater as set forth in claim 6, comprises a common timer for activating the unloading means and for the formation ~~on~~ of an overrun pulse for the locking means.

8. (Original) The bus-repeater as set forth in claim 1 adapted to transmit signal pulses received by the first bus without intermediate storage in the second bus and vice versa.

9. (Original) The bus-repeater as set forth in claim 1 adapted to re-receive signal pulses, respectively transmitted by it, in the first and the second bus.

10. (Original) The bus-repeater as set forth in claim 1, wherein the first and the second buses are CAN buses.

11. (Original) The bus-repeater as set forth in claim 10, wherein during the transmission of a dominant signal pulse received from the first bus via the second bus the locking means are activated and vice versa.

12. (Currently Amended) The bus-repeater as set forth in claim 10, wherein ~~the~~ unloading means are activated on transition from a dominant signal level to a recessive signal level.

13. (Original) The bus-repeater as set forth in claim 1, wherein the locking means comprise at least one first and one second OR gate for mutual latching, a first input of the first OR gate is connected with a receive output of the first transmit-receive means and a first input of the second OR gate is connected with a receive output of the second transmit-receive means and the output of the second OR gate is at least indirectly connected with a second input of the first OR gate and the output of the first OR gate is at least indirectly connected with a second input of the second OR gate.

14. (Currently Amended) The bus-repeater as set forth in claim 1, said bus-repeater ~~being~~ is designed in the form of an integrated circuit package.

15. (Original) A bus connection plug including a bus-repeater as set forth in claim 1.